International Conference on Spin Shuttling 2026

ICOSS 2026

September 3 (Thu.)

Songdo ConvensiA, Incheon, Korea

Abstract Book

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International Conference on Spin Shuttling (ICOSS) 2026

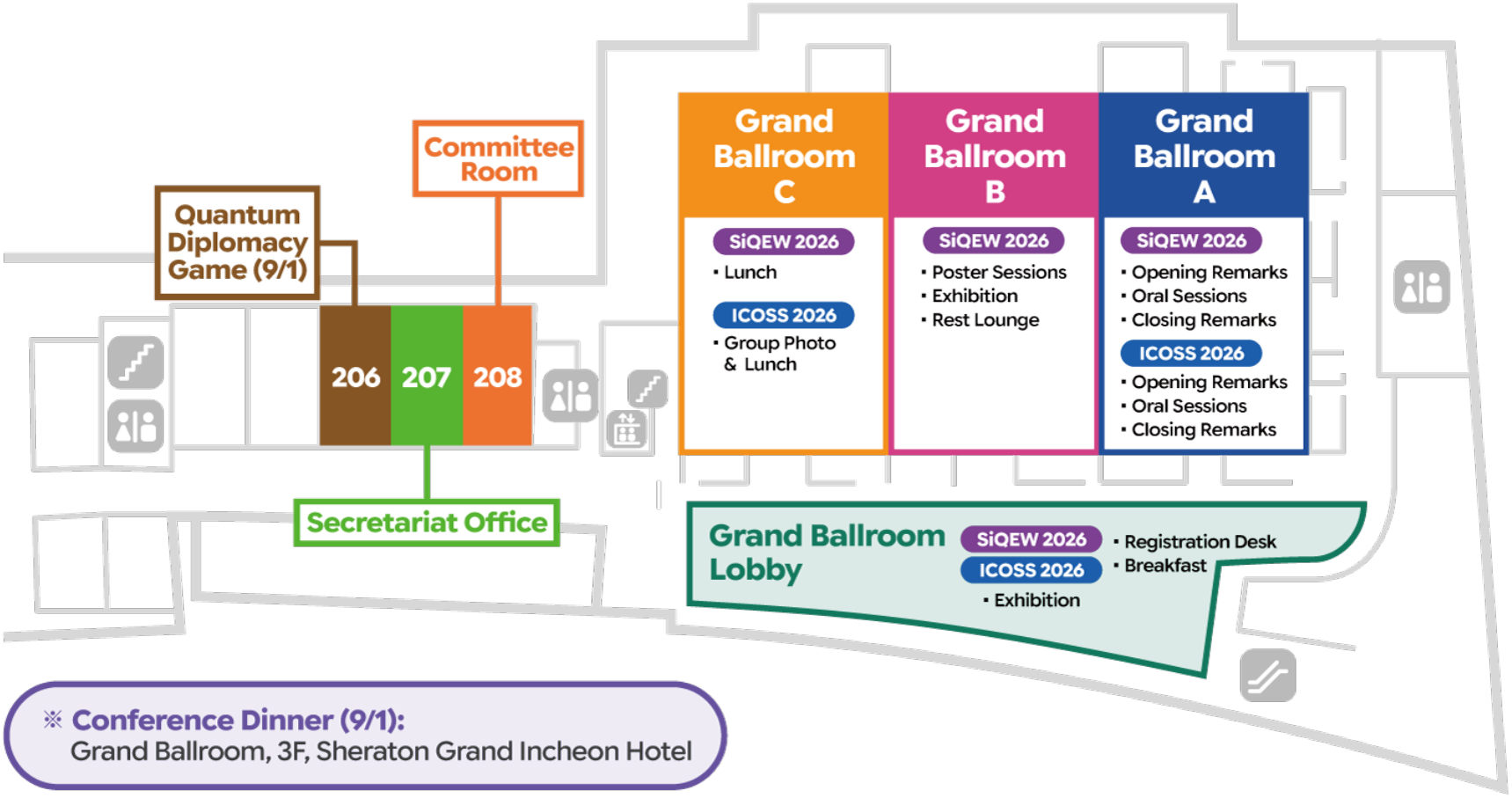
September 3 (Thu.)				Grand Ballroom A
08:00-08:25	25'	Breakfast (Lobby, 2F)		
08:25-08:30	05'	Opening Remarks		
Session I				
Session Chair: Anthony Sigillito (University of Pennsylvania, USA)				
08:30-09:15	45'	Keynote	Łukasz Cywiński (Polish Academy of Sciences, Poland)	Coherent Shuttling Spins in Silicon: A Theoretical Perspective
09:15-09:40	25'	1119	Max Beer (Forschungszentrum Jülich GmbH and RWTH Aachen University, Germany)	Scalable, High-Fidelity Operation of a T-Junction for 2D Connected Quantum Processor Architectures
09:40-10:05	25'	1056	Marcin Kepa (QuTech and TU Delft, Netherlands)	Coherent 10 μm Shuttling Link for Scalable Spin Qubit Processors
10:05-10:25	20'	Break		
Session II				
Session Chair: Mark Gyure (University of California, USA)				
10:25-10:50	25'	1128	Christian Walter Binder (University of Oxford and Quantum Motion, UK)	Using the Virtual Spin-Qubit Lab to Understand Shuttling
10:50-11:15	25'	1075	Bassil Alaeddin (University of Cambridge and Quantum Motion, UK)	Spin Shuttling along Linear Arrays of Quantum Dots in SiMOS Devices
11:15-11:40	25'	1050	Zarije Ademi (TU Delft, Netherlands)	Distributing Entanglement between Distant Germanium Qubit Registers via Shared-Control Shuttling
11:40-12:05	25'	1059	Daniel Q. L. Nguyen (TU Delft, Netherlands)	Suppressing Spin Qubit Decoherence during Shuttling via Confinement Modulation
12:05-13:30	85'	Group Photo + Lunch (Grand Ballroom C)		
Session III				
Session Chair: Xuedong Hu (University at Buffalo, USA)				
13:30-14:15	45'	Keynote	Stephen Lyon (Princeton University, USA)	Efficient Parallel Shuttling of Electron Spin Qubits Above Helium-filled Micro-Channels
14:15-14:40	25'	1098	Gordian Fuchs (Princeton University, USA)	Efficient Shuttling of Individual Electrons Bound to Liquid Helium in a CMOS Foundry-Fabricated Device
14:40-15:05	25'	1188	Heejun Byeon (EeroQ Corporation, USA)	High-Fidelity Long-Distance Shuttling of Electrons on Helium in a CCD-Like Transport Architecture
15:05-15:25	20'	Break		
Session IV				
Session Chair: Andrew Fisher (University College London, UK)				
15:25-15:50	25'	1179	Kathrin F. Koenig (Forschungszentrum Jülich GmbH and RWTH Aachen University, Germany)	Long-Distance and High-Speed Electron Shuttling in Industrially-Fabricated Si/SiGe Shuttle Devices
15:50-16:15	25'	1016	Ryo Nagai (Hitachi Ltd., Japan)	Smooth Velocity Shuttling for Suppressing Non-Adiabatic Excitations
16:15-16:45	25'	1023	Pau Dietz Romero (Forschungszentrum Jülich and IceCirc GmbH, Germany)	Valley-Aware Optimal Control for High-Fidelity Spin Shuttling with Cryogenic Integrated Electronics
16:45-16:50	05'	Closing Remarks		

FLOOR MAP

SiQEW 2026 & ICOSS 2026

SiQEW 2026
Aug. 31 - Sep. 2, 2026

ICOSS 2026
Sep. 3, 2026



※ **Conference Dinner (9/1):**
Grand Ballroom, 3F, Sheraton Grand Incheon Hotel

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I. Organizers

- **Organizing Committee**
  - Mark Friesen (University of Wisconsin–Madison, USA)
  - Lars Schreiber (JARA Institute for Quantum Information, Germany)

- **Scientific Program Committee**
  - Guido Burkard (University of Konstanz, Germany)
  - Łukasz Cywiński(Institute of Physics, Polish Academy of Sciences, Poland)
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  - Lars Schreiber (JARA Institute for Quantum Information, Germany)
  - Inga Seidler (IBM Research Europe - Zurich, Switzerland)
  - Lieven Vandersypen (QuTech and TU Delft, Netherlands)

II. Conference Information

**SiQEW 2026 and ICOSS 2026 are being held jointly this year, sharing the same official website and conference venue. Please note that SiQEW 2026 will conclude on September 2 (Wed.), and only ICOSS 2026 will take place on September 3 (Thu.).

- **Conference Website and Contact Information**

Website	siqew2026.com
General Inquiries	secretariat@siqew2026.com
Registration Inquiries	registration@siqew2026.com

- **Secretariat Office**
  - Location: Room 207, 2F, Songdo ConvensiA
  - Operating Hours

Date	August 31 (Mon.)	September 1 (Tue.)	September 2 (Wed.)	September 3 (Thu.)
Time	08:00-18:00	08:00-18:00	08:00-18:00	08:00-17:00

- **Registration Desk**
  - Location: Lobby, 2F, Songdo ConvensiA
  - Operating Hours

Date	August 31 (Mon.)	September 1 (Tue.)	September 2 (Wed.)	September 3 (Thu.)
Time	08:00-18:00	08:00-15:30	08:00-17:30	08:00-17:00

  - On-site Registration Fee

※ Credit cards and Cash are the only accepted forms of payment for on-site registration.

Category	Type	On-site August 31 (Mon.)- September 3 (Thu.)	Registration Fee Includes
SiQEW (Aug. 31 ~ Sep. 2)	Regular	USD 850	All Scientific Sessions, Daily Breakfast, Coffee Breaks, Lunches, and One Conference Dinner
	Student		
ICOSS (Sep. 3)	Regular	USD 180	All Scientific Sessions, Breakfast, Coffee Breaks, and Lunch
	Student		
SiQEW & ICOSS (Aug. 31 ~ Sep. 3)	Regular	USD 1,030	All Scientific Sessions, Daily Breakfast, Coffee Breaks, Lunches, and One Conference Dinner
	Student		

II. Conference Information

- **Name Badge**

For security purposes, all participants are required to wear their name badges throughout the conference. If your badge requires any correction, please visit the registration desk for a replacement. Staff will be stationed at the entrances to all session rooms to check badges.

- **Breakfast**

- Location: Grand Ballroom Lobby, 2F, Songdo ConvensiA
- Operating Hours

Date	August 31 (Mon.)	September 1 (Tue.)	September 2 (Wed.)	September 3 (Thu.)
Time	08:00 - 08:40	08:00 - 08:55	07:55 - 08:55	08:00 - 08:25

- **Lunch**

- Location: Grand Ballroom C, 2F, Songdo ConvensiA
- Operating Hours

Date	August 31 (Mon.)	September 1 (Tue.)	September 2 (Wed.)	September 3 (Thu.)
Time	12:50-13:50	12:50-13:50	12:50-14:00	12:05-13:30

- **Rest Lounge & Coffee Break**

- Location: Grand Ballroom B, 2F, Songdo ConvensiA
- Operating Dates: August 31 (Mon.) - September 2 (Wed.)

A Rest Lounge and Coffee Break area will be available in Grand Ballroom B. Take a break and enjoy a variety of popular Korean ice creams!

**On September 3 (Thu.), the Rest Lounge and Coffee Break area will be located in the lobby.

- **WiFi Facility**

- Free Wifi is provided inside Songdo ConvensiA for the convenience of visitors and conference attendees.

▶ WiFi ID: Free_ConvensiA

- **General Information**

Conference Venue	Around Songdo ConvensiA
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III. Sponsors

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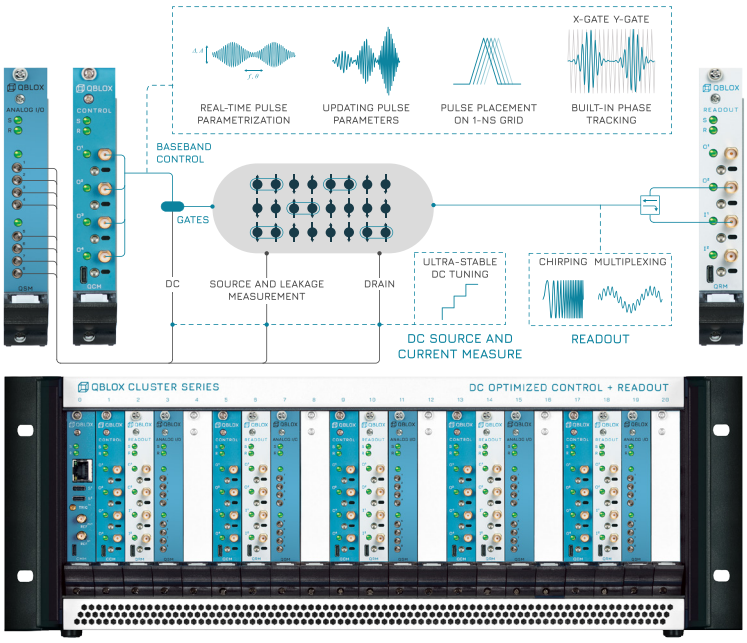

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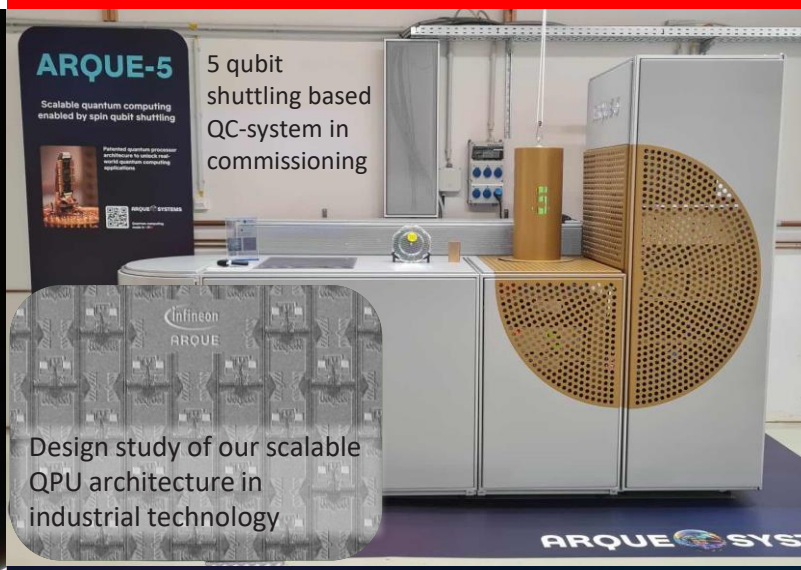

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IV. Presentation Guidelines

- **Contributed Oral Presentation**
  - SiQEW: 20min. (including Q&A) / ICOSS: 25min. (including Q&A)
  - Authors of abstracts accepted for oral presentation are requested to prepare their presentation slides in Microsoft PowerPoint or PDF format using a 16:9 aspect ratio.
  - Presenters should deliver their presentations from the podium using the computer provided in the session room.
  - To prevent software compatibility issues, presenters are advised to save their presentation file on a USB flash drive and bring a backup copy.
  - Using a personal laptop, particularly a MacBook, is not recommended unless the presentation requires specific software or hardware.
  - Presentation files should be uploaded to the computer in the assigned session room during the break before the session.

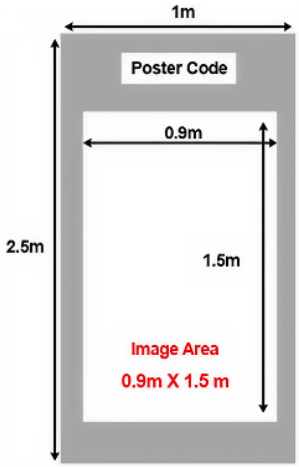
- **Contributed Poster Presentation**

  Poster Presentation
  - Poster authors are responsible for preparing, printing, and transporting their posters to the conference venue.
  - Please note that poster printing services will not be available on-site.
  - Please mount your poster on the presentation board corresponding to your assigned presentation code.
  - Tape, thumbtacks, and scissors will be provided by the Secretariat.
  - Authors are requested to remove their posters during the designated poster removal time. Any posters remaining after the removal period will be discarded by the Secretariat.

Place: Grand Ballroom B	Poster Session I (August 31 (Mon.))	Poster Session II (September 1 (Tue.)) ** ICOSS Poster
Put-up	08:00-15:30	08:00-13:30
Presentation	16:00-17:40	14:00-15:40
Take-down	17:40-18:30	15:40-19:00

Poster Specifications

- Panel Size: 1m (W)*2.5m (H)
- Poster Size: (Maximum size) 0.9 m(W) × 1.5 m(H)
- Each poster should indicate the paper title, authors, and affiliation.



Keynote I September 3 (Thu.) 08:30 - 09:15

Coherent shuttling spins in silicon: a theoretical perspective

Łukasz Cywiński[1]

[1]*Institute of Physics, Polish Academy of Sciences, Warszawa, Poland*

The idea of using long-distance shuttling of spin qubits as a crucial element of scalable architectures has been around since 2005 [1], but it took some time for this idea to become sufficiently embraced that we could gather at a conference devoted entirely to spin shuttling. Moving spin qubits across 1–10 micron distances is now being achieved in many laboratories, and mastering this technique provides not only a means of transferring quantum information, but also new tools for large-area mapping of properties of the underlying nanostructure, such as valley splitting [2,3] and g-factor [4].

I will recount how realistic modeling of electron transport in bucket-brigade and conveyor-belt scalable designs [5,6] gave us reason for optimism regarding the prospects of coherent spin shuttling a few years ago, and how subsequent experimental results led to refinement of theoretical models of decoherence during shuttling [3]. The question of adiabaticity versus nonadiabaticity — in charge, valley, and spin dynamics — will be a recurring theme. I will also discuss insights into valley splitting [2,3], g-factor [4,7], and valley coupling [4] disorder that emerge from device characterization via shuttling.

I would like to thank Lars Schreiber for inviting me in 2017 to work on this fascinating topic. Our initial joint work was supported by the QuantERA programme (project Si-QuBus). I acknowledge current support from the European Union's Horizon 2020 Research and Innovation Actions under Grant Agreement No. 101174557 (QLSI2).

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[1] J.M. Taylor, et al., Nature Physics **1**, 277 (2005).

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[5] Langrock, J.A. Krzywda, et al., PRX Quantum **4**, 020305 (2023).

[6] J. A. Krzywda and Ł. Cywiński, Phys. Rev. B **101**, 035303 (2020); **104**, 075439 (2021); **111**, 115305 (2025).

[7] Ł. Cywiński et al., arXiv:2604.24689 (2026).

Oral | September 3 (Thu.) 09:15-09:40

Scalable, high-fidelity operation of a T-junction for 2D connected quantum processor architectures

M. Beer[1], S. Majumder[2], S. Trellenkamp[3], J. S. Tu[3], H. Bluhm[1,4], J. Knoch[2], and L. R. Schreiber[1,4]

[1]*JARA-FIT Institute for Quantum Information, Forschungszentrum Jülich GmbH and RWTH Aachen University, Aachen, Germany*

[2]*Institute of Semiconductor Electronics, RWTH Aachen University, Aachen, Germany*

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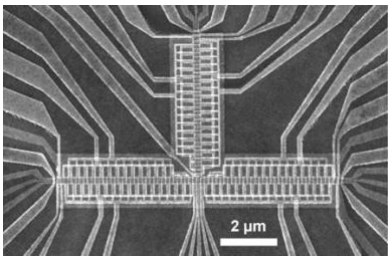
[4]*ARQUE Systems GmbH, 52074 Aachen, Germany*

Conveyor mode qubit shuttling provides a scalable method to coherently transport electron spin qubits over large distances and thus provides means to entangle far-distant qubits [1,2,3]. In addition, only few signal channels are required independent from length, which reduces the signal fanout complexity [4]. But a scalable quantum computing architecture requires further improvements in terms of qubit routing [5] and simplification of control electronics.



The T-junction. Scanning electron micrograph of the 54 quantum dot device (from [6]).

We demonstrate electron routing in a conveyor mode T-junction device consisting of two perpendicular, independent shuttling channels spanning 54 quantum dots using sinusoidal voltage signals of identical amplitude and offset [6]. Despite the substantial difference in device geometry in the junction, in contrast to the linear shuttle channels, transfer between perpendicular channels is achieved by operating each conveyor as done during linear shuttling.

Going beyond Ref. [6], we show that shuttling pulses can be centered around 0 V by biasing all charge injecting ohmic contacts with the same constant voltage offset. By this bias lift we can eliminate bulky bias-tees, reducing line count and improving AC signal integrity. This is achieved maintaining the high fidelity of conveyor mode charge shuttling previously demonstrated [4,6] with a fidelity of 99.9996 % per transfer at 280 mm/s. Furthermore, the shuttle architecture provides enough space to integrate an asymmetric sensing dot (ASD) replacing the usual charge detector [7]. The ASD enables direct baseband readout of the voltage across the sensor, in contrast to more demanding current readout. The large bias-swing of the ASD potentially allows on-chip amplification of the detection signal by a co-integrated high electron mobility transistor (HEMT).

References

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3. Matsumoto et al. arXiv:2503.15434 (2025).
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Oral | September 3 (Thu.) 09:40-10:05

Coherent 10 µm shuttling link for scalable spin qubit processors

Marcin Kepa[1], Yuta Matsumoto[1], Maxim De Smet[1], Davide Degli Esposti[1], Sander de Snoo[1], Giordano Scappucci[1], Lieven M.K. Vandersypen[1]

[1]*QuTech, TUDelft, Lorentzweg 1, 2628 CJ Delft, Netherlands*

Long-range coherent links between spin qubits are a necessary ingredient for quantum processor architectures based on sparsely connected registers [1]. This approach relaxes constraints on crosstalk and fanout and enables classical electronics integration. Links based on micron-scale shuttling have been demonstrated in germanium within a 1.25 µm long channel [2] and in silicon with charge transport over 10 µm [3]. Here, we demonstrate spin qubit transport across a 10 µm channel, preserving arbitrary spin states with an estimated 98% fidelity. Electrons are propelled in traveling-wave potentials induced by 143 shared-control gates on top of a Si/SiGe quantum well. We extend the scheme to multi-electron operation by using the conveyor as a shift register, sequentially loading, initialising spin, shuttling, and reading out the spin polarisation. The channel can thus serve as a storage zone during computation or as a multiplexed readout line for a qubit array. Together, this could serve as a unit cell of an architecture consisting of static dot registers, fanout-efficient coherent links, memory and readout zones.

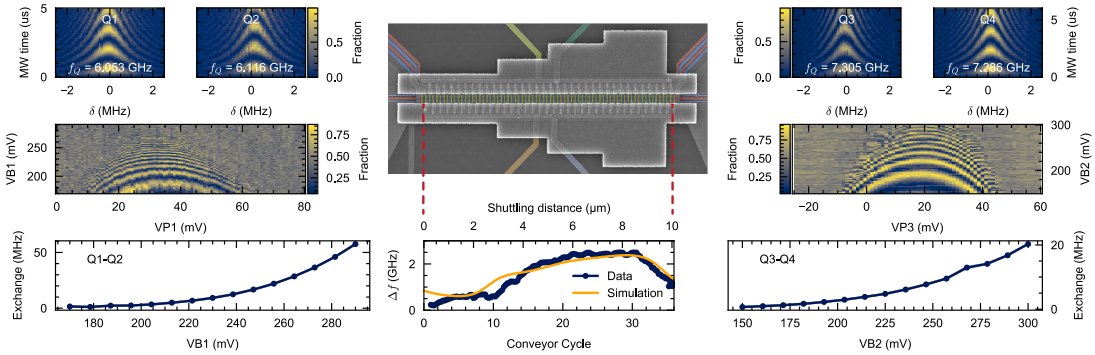

Fig. 1. False-colored SEM image of the device with chevron patterns, fingerprint scans of exchange oscillations and extracted exchange tunability of left and right static dot pairs. Static pairs are connected by a shared-control shuttling channel with a micro-magnet placed on top of the channel inducing a position-dependent Zeeman splitting. This dependency is probed by Ramsey experiments with variable wait time at each position inside the conveyor. The detuning with respect to the static dot frequency is extracted from the resulting oscillations and plotted in the bottom middle panel.

Reference list

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2. Ademi, Z. et al. Distributing entanglement between distant semiconductor qubit registers using a shared-control shuttling link. Preprint at: arXiv:2510.26860.
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Oral | September 3 (Thu.) 10:25-10:50

Using the virtual spin-qubit lab to understand shuttling

C. W. Binder[1,2], J. J. Turner[2], L. Peri[2], G. Burkard[3], A. J. Fisher[4,2], and S. C. Benjamin[1,2]

[1]*Department of Materials, University of Oxford, Parks Rd, Oxford OX1 3PJ, UK*

[2]*Quantum Motion, 9 Sterling Way, London N7 9HJ, UK*

[3]*Department of Physics, University of Konstanz, D-78457 Konstanz, Germany*

[4]*Department of Physics and Astronomy and London Centre for Nanotechnology, University College London, London WC1E 6BT, UK*

Over the past two years we have developed a virtual spin-qubit laboratory for fast, realistic simulation of silicon-based quantum-dot devices. A recent effort has made the framework platform-agnostic: the same pipeline now handles electrons and holes in Si/SiO_2, Si/SiGe and Ge/SiGe heterostructures, including multi-particle systems. The underlying solvers have become fast enough that fully time-dependent simulation of large devices is now easily possible, and we have furthermore recently added spin-orbit coupling to the eigensolvers. Our novel capabilities give us the possibility to look at a suite of shuttling and other time-dependent phenomena across semiconductor-based quantum computing. We begin with single-electron conveyor-belt shuttling in Si/SiO_2 and Si/SiGe, and calculate valley landscapes, excitation and relaxation rates (and their impact on decoherence) for both platforms. We then focus on richer encodings, such as dual-spin qubits, and quantify their advantage over their conventional Loss-DiVincenzo counterparts. We also take a brief look at shuttling of multi-electron systems, where we examine possible leakage pathways. Finally, we explore *gates while shuttling*: driving single-qubit operations via micromagnet stray fields in Si/SiGe during transport, thereby examining more exotic shuttling-and-control workflows across platforms. As a natural by-product, the same time-dependent machinery also lets us study phenomena such as valley qubits in their dynamical regime. Every simulation we show is performed on realistic device geometries — including atomic-scale interface roughness, Si/Ge alloy disorder, charged interface defects, and micromagnet stray fields. This allows us to virtually replicate current experiments and explore room for further optimization. Built on a single fast toolkit with a visualisation layer that lets one look inside the device at every step, the aim is to give the shuttling community a broad, concrete picture of where modern silicon-spin-qubit simulation now stands and how it could be improved.

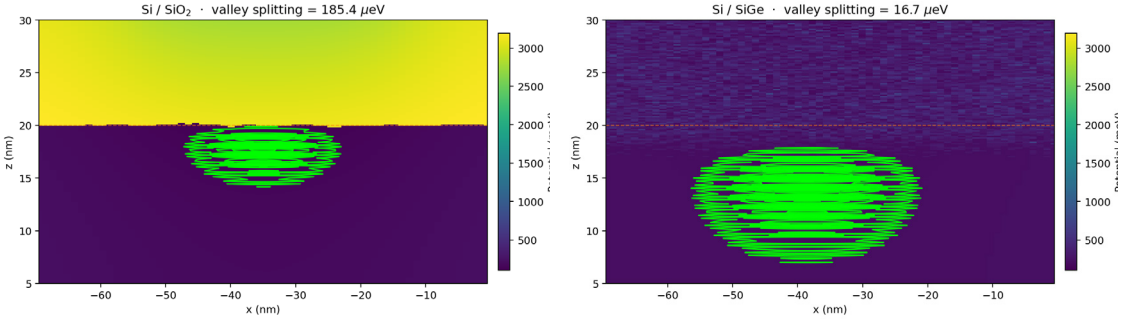

Figure 1. Cross-section of a single-electron eigenstate in the same device geometry, simulated on two platforms within the framework. Left: Si/SiO₂, where the sharp oxide barrier ($z \approx 20$ nm) yields a valley splitting of 185.4 μeV. Right: Si/SiGe, where the alloy disorder of the SiGe barrier — visible as the speckled potential above the dashed interface — reduces the valley splitting on this disorder realisation to 16.7 μeV. Green contours show the electron probability density $|\psi|^2$, and the colour map shows the electron potential energy.

References

• C. W. Binder and S. C. Benjamin, Nature Nanotechnology 20, 857–858 (2025). DOI: 10.1038/s41565-025-01942-z.

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Oral | September 3 (Thu.) 10:50-11:15

Spin shuttling along linear arrays of quantum dots in SiMOS devices

Bassil Alaeddin[1,2], Giovanni A. Oakes[2], Lorenzo Peri[2], Jack J. Turner[2], Christian W. Binder[3,2], David J. Ibberson[2], Keith Muir[2], April Carniol[2], Sofie Beyne[4], Danny Wan[4], Julien Jussot[4], Stefan Kubicek[4], Kristiaan DeGreve[4], Andrew J. Fisher[5,2], Christopher J. B. Ford[1], John J. L. Morton[2] and M. Fernando Gonzalez-Zalba[2,6,7]

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Spin qubits in silicon quantum dots (QDs) are a promising platform for quantum computation due to their compatibility with CMOS fabrication processes, long coherence times and potential for scalable architectures [1]. Electron spin shuttling offers a route to improved qubit connectivity with two primary approaches: bucket-brigade, which transfers electrons sequentially between static QDs, and conveyor-mode, which transports electrons using a smoothly moving wave potential [2]. Coherent spin shuttling in silicon-germanium (Si/SiGe) devices has been shown along linear arrays of multiple QDs [3, 4], but demonstrations of spin shuttling in silicon-oxide (SiMOS) devices have so far been limited to double quantum dot (DQD) experiments [5, 6]. Here we study bucket-brigade shuttling in a SiMOS device comprising a linear array of four QDs with adjacent single-electron transistors (SETs) for charge sensing. Spin shuttling was demonstrated along the array (Fig. 1(a) and 1(b)) using electron spin resonance (ESR) control and Pauli spin blockade-based readout, enabling tuning of site-dependent g-factor and Rabi frequency. Through analysis of shuttling speeds to maximise performance, shuttling over a cumulative distance greater than 10 µm at an average velocity above 2.5 m/s was achieved whilst maintaining spin eigenstate fidelities above 99.4% per shuttle hop. Ramsey interferometry measurements demonstrate the level of phase coherence preserved and allowed for accurate mapping of Larmor frequencies and valley excitations along the array. Building on these results, and by leveraging novel 3D modelling simulations of conveyor-mode shuttling in SiMOS devices to optimise gate pulses and shuttling fidelity [7], we study spin shuttling along longer QD arrays, indicating the feasibility of long-range coherent spin shuttling and enhancing prospects for future large-scale fault-tolerant quantum processors in SiMOS platforms.

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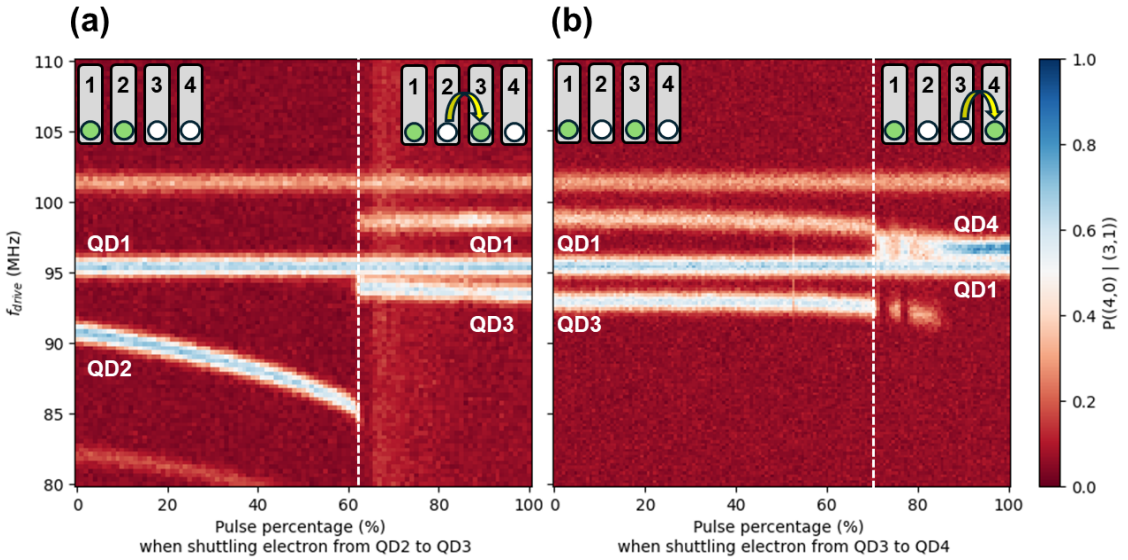

Fig. 1: Spin shuttling in a SiMOS device comprising a linear array of four quantum dots (QDs). In (a) and (b), plots are shown of the probability an electron spin has flipped after applying a π microwave pulse, as a function of the electron spin resonance (ESR) drive frequency, f_{drive}, and the pulse percentage when shuttling an electron between pairs of QDs: (a) QD2 to QD3 and (b) QD3 to QD4; abrupt changes in the resonant ESR frequency under different voltage pulse levels indicate the electron has shuttled from one QD to the next.

Oral | September 3 (Thu.) 11:15-11:40

Distributing entanglement between distant Germanium qubit registers via shared-control shuttling

Z. Ademi[1]*, M. Bassi[1]*, C. X. Yu[1], S. L. de Snoo[1], Y. Matsumoto[1], S. D. Oosterhout[2], A. Sammak[2], L. Vandersypen[1], G. Scappucci[1], C. Déprez[1] and M. Veldhorst[1]

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Spin qubits in semiconductor quantum dots [1] hold great promises for building large-scale quantum computers. With high-fidelity qubit control already achieved in rudimentary linear and two-dimensional spin qubit arrays [2, 3], challenges such as wiring density and qubit-to-qubit interconnectivity limit further scaling. One way to address these challenges is to interconnect medium-sized qubit registers via shuttling links [4], encouraged by the recent demonstrations of high-fidelity shuttling [5], electron spin teleportation and multi-qubit entanglement in silicon devices [6-8].

While these results highlight the promise of shuttling architectures, scaling beyond individually wired gates and realizing conveyor-mode shuttling, particularly for hole spin qubits with strong spin–orbit coupling, remain open challenges. Here, we demonstrate coherent transfer of a single hole spin between two germanium qubit registers spaced more than one micron apart using a shared-control conveyor-mode shuttling link, see Fig. a.). Combining shuttling with resonant control, we correct for spin rotations induced by spin-orbit interaction during transport and show remote entanglement of a Bell state between two spins distributed into distant registers [9]. The resulting density matrices of each Bell state, measured by quantum state tomography, are depicted in Fig. b.-d.). These findings highlight the potential of conveyor-mode shuttling with minimal gate wiring overhead for advancing modular hole-spin-based quantum processors.

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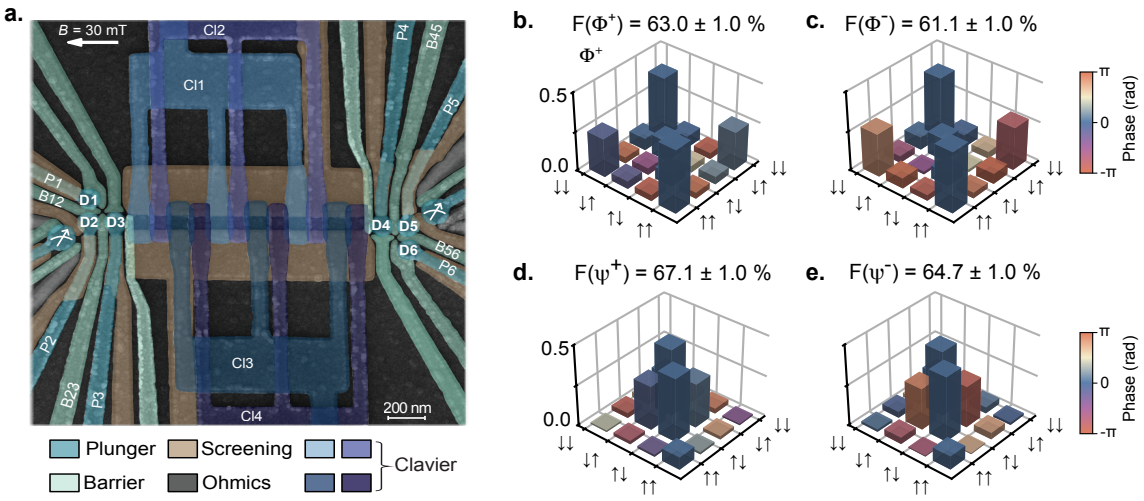

Figure. a.) False-colored SEM of a modular quantum device, including a 1.2 µm long shuttling lane that connects two qubit registers, each comprising 3 dots and a charge sensor **b.) – e.)** Reconstructed density matrices of the four Bell states and corresponding bare state fidelities assessing remote entanglement generation while shuttling the spin from one register to the other.

Oral | September 3 (Thu.) 11:40-12:05

Suppressing spin qubit decoherence during shuttling via confinement modulation

Daniel Q. L. Nguyen[1], Maximilian Rimbach-Russ[1], Stefano Bosco[1]

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Reliable long-range qubit shuttling is a powerful tool for scalable quantum computing architectures[1,2,3]. We investigate strategies to improve the coherence of moving spin qubits by performing continuous dynamical decoupling[4] by modulating their confinement potential. Specifically, we introduce temporal and spatial breathing shuttling protocols that leverage spin-orbit interactions in hole-spin systems to electrically drive the qubit while moving. This enables efficient dressed-state shuttling, where the spin is continuously rotated during transport, suppressing the effect of low-frequency noise. Using the filter function formalism, we identify driving regimes that efficiently mitigate both global and local magnetic and electric noise sources. We find that confinement-modulated shuttling can significantly enhance coherence during transport, while revealing distinct limitations depending on the correlation length of the noise. Applying our framework to germanium hole-spin qubits, we show that these protocols provide a practical route toward noise-resilient long-range coherent quantum links

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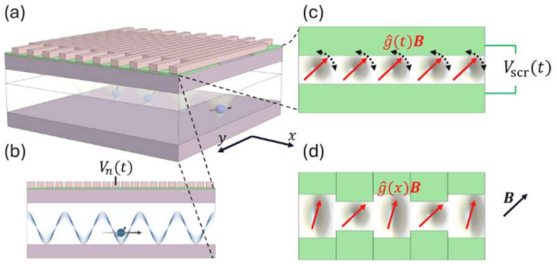
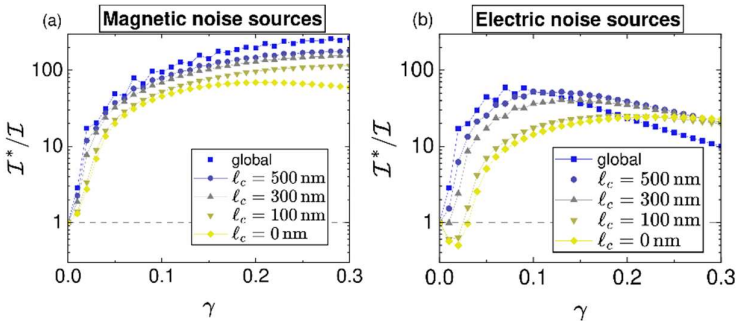


Schematic. (a) Conveyor-mode shuttling architecture. (b,c) Temporal breathing via modulation of the top-gate or screening-gate potentials. (d) Spatial breathing via periodic screening-gate design, producing time-dependent confinement during constant-velocity shuttling.



Numerical simulation. Ratio I^*/I comparing infidelity without (I^*) and with (I) temporal confinement modulation. Panels (a,b) show the dependence on the driving amplitude γ for magnetic and electric noise sources of varying spatial correlation lengths.

Keynote I September 3 (Thu.) 13:30-14:15

Efficient Parallel Shuttling of Electron Spin Qubits Above Helium-filled Micro-Channels

S. A. Lyon[1,2]

[1]*Princeton University, USA,*

[2]*EeroQ Corp., USA*

Key potential advantages of electron spin qubits over other quantum processor technologies include the facts that electrons are small, light, and highly mobile. Charge-coupled devices (CCDs) have demonstrated GHz speeds in semiconductors, and are capable of moving arrays of millions of electrons simultaneously over prescribed paths with only a few control lines. They naturally lend themselves to highly parallel quantum error correction and computing architectures. However, moving electrons inside a semiconductor introduces the possibility of spin decoherence through the spin-orbit interaction. Shuttling electrons across a superfluid helium surface is expected to largely eliminate this decoherence, and I will discuss calculations which find that spin-orbit decoherence is negligible for electrons bound to helium. I will also discuss experiments demonstrating the choreographed motion of about 4000 small electron packets (down to an average of 1 electron per packet) in a device which was produced in a CMOS foundry. In other recent experiments, individual electrons have been isolated, and then shuttled along paths for millimeters in foundry fabricated devices. These results provide strong evidence for the viability of shuttling large arrays of individual electron spin qubits in this technology.

Oral | September 3 (Thu.) 14:15-14:40

Efficient shuttling of individual electrons bound to liquid helium in a CMOS foundry-fabricated device

Gordian Fuchs[1], Tiffany Liu[1], Mayer M. Feldman[1,2,3], Michael D. Henry[4], Eric A. Shaner[4], Luke A. D'Imperio[4], and Stephen A. Lyon[1,5]

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Despite previous progress on shuttling small packets of electrons across multiple parallel, gate-defined, helium-filled microchannels, realizing single electron transport on CMOS foundry-fabricated devices has so far remained elusive [1,2]. Here, we demonstrate charge shuttling of individual electrons over distances of several mm including rapidly transferring between vertical and horizontal channels via T-junctions using 3-phase CCDs. Six horizontal channels, each containing a sensing section, feed into a ~4 mm long vertical CCD, with electrons shuttled along and between these CCDs. The shuttling speed in these devices is currently only limited by the wiring in the dewar. A unique set of gates at the end of a 177 µm long horizontal CCD section, labelled "Electron Storage" in the figure below, is used to store an electron and identify which of the 6 parallel horizontal channels it occupies. Electron sensors, operating at a modulation frequency of 1 MHz, are located in the horizontal channels and allow us to measure as few as a single electron using a bespoke cryogenic pre-amplifier circuit without the need for superconducting single electron transistors (SETs) or a tuned rf resonator [3,4]. The microchannel devices were fabricated using a complementary-metal-oxide-silicon (CMOS) multilayer back-end-of-line (BEOL) process at the Sandia National Laboratories MESA fab.

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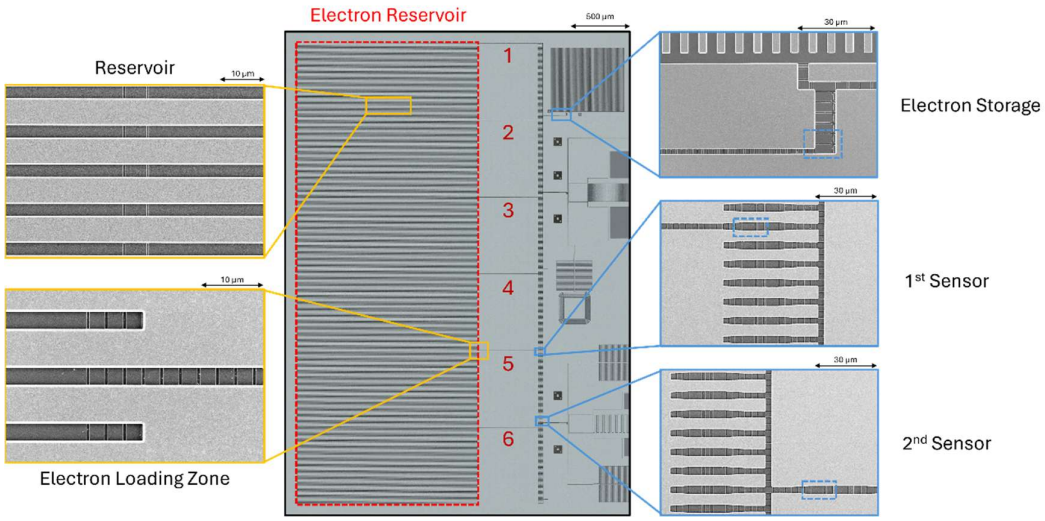

Figure. Optical and SEM images of the microchannel device showing different regions including 6 numbered horizontal channels and a ~4 mm long vertical channel for loading, shuttling, sensing, and storing electrons.

Oral | September 3 (Thu.) 14:40-15:05

High-fidelity long-distance shuttling of electrons on helium in a CCD-like transport architecture

Heejun Byeon, Kyle E. Castoria, Niyaz R. Beysengulov, Michael Sammon, Abhilasha Ramesh, Johannes Pollanen, David G. Rees, and Stephen A. Lyon

EeroQ Corporation, Chicago, Illinois, USA

Electrons trapped above the surface of superfluid helium are attractive candidates for mobile spin qubits due to their predicted long coherence times and exceptional mobility. Scalable quantum computing architectures based on this system require reliable transport of electrons over long distances with minimal loss during repeated shuttling operations. Here, we investigate electron shuttling in a CCD-like architecture integrated with 128 parallel microchannels fabricated using a CMOS foundry process. Electrons are shuttled between reservoir and detection regions using CCD-style transfer operations, in packets ranging from several tens down to single electrons. Repeated transport experiments demonstrate robust shuttling over more than one million transfer cycles, corresponding to cumulative travel distances approaching 100 meters, with no measurable electron loss. These results highlight the robustness of repeated electron shuttling on superfluid helium and support the feasibility of scalable spin-qubit architectures based on electron on helium.

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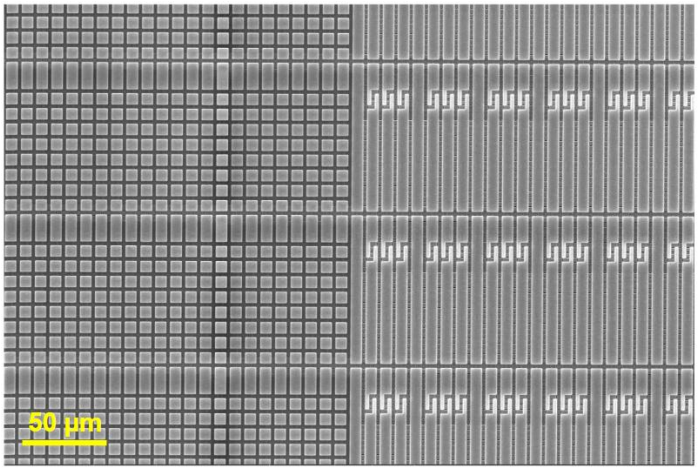

Figure 1. SEM image of the CCD-like electron shuttling architecture fabricated using a CMOS foundry process. Left: electron reservoirs. Right: electron detection region.

Oral | September 3 (Thu.) 15:25-15:50

Long-distance and high-speed electron shuttling in industrially-fabricated Si/SiGe shuttle devices

A.Sala[1,2], J. Sehringer[1,3], P. Muster[3], W. Langheinrich[3], S. Pregl[3], K. F. Koenig[1], L. Schreiber[1,2], and H. Bluhm[1,2]

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[2]*ARQUE Systems GmbH, 52074 Aachen, Germany*

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Electron shuttling is being explored as a possible mechanism for scaling semiconductor spin-qubit architectures by enabling the transfer of quantum information between spatially separated sites [1–3]. A key requirement is the preservation of spin coherence during transport, which can be limited both by localized disorder in the shuttling channel, such as electrostatic inhomogenities or defects in the Si/SiGe heterostructure, and by global noise processes that accumulate over the shuttling time [2, 4]. While localized disorder may require larger driving amplitudes or reduced shuttling velocities to maintain reliable transport, decoherence from electric and magnetic noise may be mitigated by faster shuttling.

Here, we report progress on electron shuttling in an industrial Si/SiGe CMOS device [5, 6]. Using only four independent signal channels to control the electrostatic gate sequence, we investigate high-speed transport over micrometer-scale distances. Electrons are transported over single-pass distances of up to 3 μm, with measured shuttling velocities ranging from 4 mm/s to 20 m/s. Additional measurements on shorter-distance shuttling sequences access transport velocities extending into the 100 m/s regime.

By characterizing the dependence of transport on drive amplitude and frequency, we identify operational constraints for high-speed shuttling and determine the conditions required for reproducible transport trajectories and return to the initial charge configuration. Operating close to the limits of reliable transport, such as at low amplitudes or high shuttling frequencies, additionally enables disorder mapping by revealing regions of the shuttling channel that are more susceptible to transport failure.

These results contribute toward the development of scalable semiconductor spin-qubit architectures with long-range electron transport capabilities.

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Oral | September 3 (Thu.) 15:50-16:15

Smooth Velocity Shuttling for Suppressing Non-Adiabatic Excitations

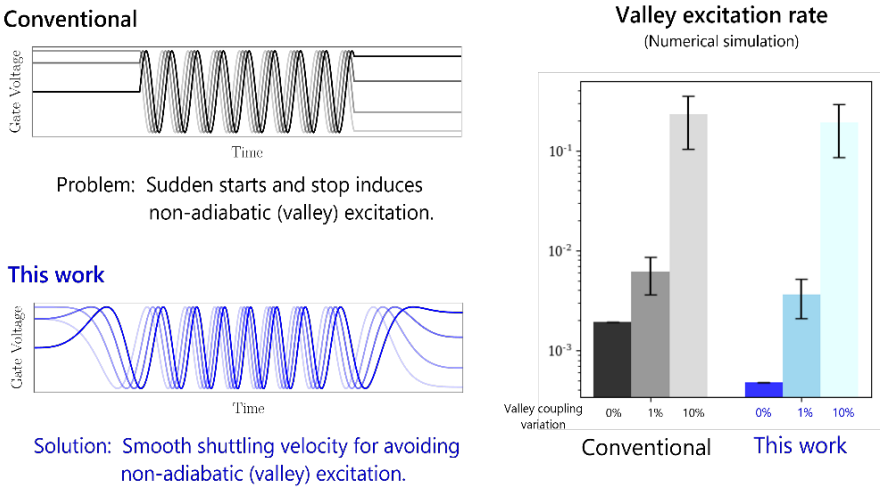
Ryo Nagai, Takashi Takemoto, and Hiroyuki Mizuno
Research and Development Group, Hitachi, Ltd., Kokubunji, Tokyo, Japan.

Implementing fault-tolerant silicon quantum computers requires robust electron shuttling, including complex operations like stopping and routing. However, conventional methods often involve abrupt starts and stops. Such rapid changes in the confining potential cause non-adiabatic transitions to higher-energy states, severely degrading qubit fidelity.

In this study, we propose *smooth velocity shuttling*. We demonstrate that by smoothing the shuttling velocity profile, non-adiabatic transitions can be significantly suppressed. Practically, this smooth velocity control can be implemented through the frequency modulation of gate voltages. Furthermore, we reveal that the problem of optimal velocity design can be mathematically identified with the design problem of window functions in signal processing.

To verify the effect of smooth velocity shuttling, we performed numerical simulations. These simulations calculated valley excitation rates while incorporating Si interface variations (0%, 1%, and 10%). The results, as shown in the right panel of the attached figure, confirm that velocity shaping indeed suppresses valley excitations. Specifically, we found that this suppression effect becomes remarkably pronounced when the Si interface variations are small. In the future, when the impact of these variations is minimized—such as through the precise tuning of quantum dot size—this proposed method will demonstrate its full potential as a key strategy for further enhancing shuttling fidelity.

This work was supported by JST Moonshot R&D, Grant Number JPMJ2065.



Oral | September 3 (Thu.) 16:15-16:45

Valley-Aware Optimal Control for High-Fidelity Spin Shuttling with Cryogenic Integrated Electronics

Pau Dietz Romero[1,6], Nermine Chaabani[2,3], Lammert Duipmans[1], Alessandro David[2], Felix Motzoi[2,3], Stefan van Waasen[1,4,6], and Lotte Geck[1,5,6]

[1]*Integrated Computing Architectures (PGI-4), Forschungszentrum Jülich, Germany*

[2]*Quantum Control (PGI-8), Forschungszentrum Jülich, Germany*

[3]*Institute for Theoretical Physics, University of Cologne, Germany*

[4]*Faculty of Engineering, Communication Systems, University of Duisburg-Essen, Germany*

[5]*System Engineering for Quantum Computing, RWTH Aachen University, Germany*

[6]*IceCirc GmbH, Germany*

Scalable spin-qubit architectures can be realized using sparse qubit-grid concepts such as SpinBus [1], combined with local cryogenic control electronics and micrometer-scale shuttling links to overcome the wiring bottleneck [2]. In Si/SiGe devices, however, spatial fluctuations in valley splitting can create regions with extremely low valley splitting that strongly reduce shuttling fidelity. Electronic noise from the local circuitry additionally results in shot-to-shot variations in the effective shuttling trajectory, further degrading the mean performance due to nondeterministic valley-spin interaction.

We present a valley-aware shuttling protocol co-designed with an ultra-low-power cryogenic signal generator, developed through an interdisciplinary effort between cryogenic electronics experts and quantum control experts. This interdisciplinary control approach is optimized and validated within a co-simulation framework that combines transistor-level simulation of cryogenic integrated circuits in Cadence Spectre with the valley-aware qubit model introduced in [3].

In the co-simulation, four phase-shifted gate signals, consistent with the SpinBus architecture [1], shuttle an electron in a traveling quantum dot, while the local valley landscape sampled by the qubit is taken into account in the optimization, as shown in Fig. 1. The optimized waveform is stored and replayed on chip using only four discrete hardware settings per signal period, enabling parallel optimization across many channels with low memory, wiring, and power overhead. In the co-simulation, we improve the shuttling fidelity for 10 µm transport at 20 m/s from 99.78 ± 0.06% to 99.99 ± 0.007%, thereby also increasing robustness against non-deterministic electronic noise while keeping active analog power below 10 µW per shuttling channel.

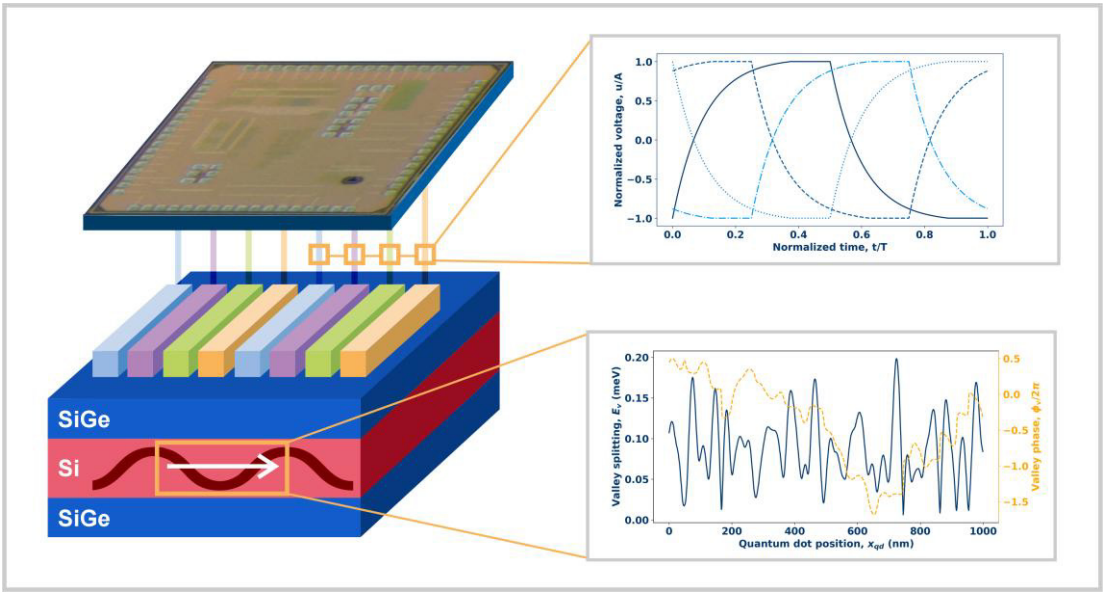


Figure 1. Shuttling concept with integrated electronics investigated in this work. Four phase-shifted gate voltages are generated in close proximity to the qubit based on optimized parameters stored on the CMOS chip. The co-simulation incorporates spatial variations in valley splitting and valley phase experienced by the moving electron. Adapted from Fig. 2 in [4].

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Poster | September 1 (Tue.) 14:00-15:40

[P2-58]

Simulations of electron shuttling with tight-binding time evolution

Wilhem Harvey[1,2], Pericles Philippopoulos[1], Raphaël J. Prentki[1], Zhanghao Zhouyin[1,3], Mohammad Reza Mostaan[1], Yu Zhu[1], Hong Guo[3], and Félix Beaudoin[1]

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[2]*Université de Sherbrooke, Sherbrooke, Canada,* [3]*McGill University, Montréal, Canada*

Shuttling, the coherent transport of electrons over microns, is a promising route to scalable spin-qubit quantum computers. Atomistic disorder limits shuttling fidelities; while its impact on valley leakage is well-understood, its impact on spin and orbital excitations is largely unexplored.

Here, we present a shuttling simulation framework [Fig.(a)] implemented in QTCAD®, which treats the charge, spin, and orbital degrees of freedom on equal footings. Using discretized time evolution of a spinful atomistic tight-binding Hamiltonian, we obtain position-resolved predictions of spin and valley-resolved leakage. This involves repeated exponentiation of 1M-by-1M sparse matrices with 10 fs time steps, enabled by novel and efficient numerical routines.

We consider shuttling at 100 m/s in SiO_2–Si–SiO_2 devices with realistic interface roughness [Fig.(b)]. For 4 Å RMS roughness, leakage is >10% [Figs.(c,e)]. For 2 Å RMS roughness, leakage is lower [Fig.(d)], but Zeeman and valley splittings are comparable, which can compromise qubit reliability. Reducing roughness to 1 Å RMS has been associated with increases in leakage[1]. Our approach enables systematic exploration of parameter regimes to balance these competing effects.

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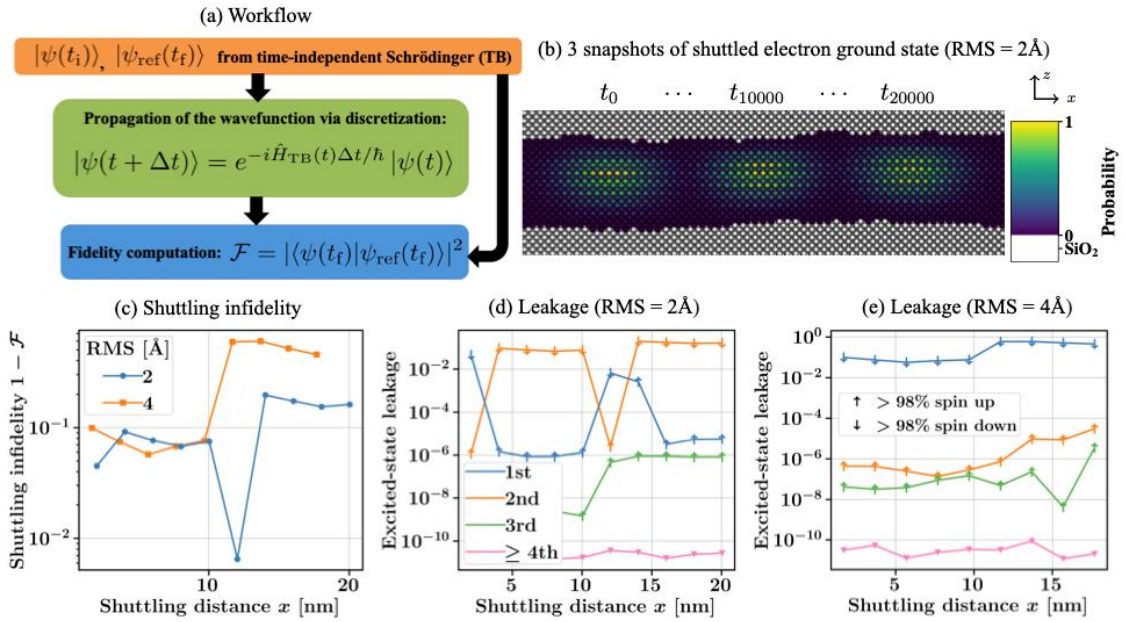

Poster | September 1 (Tue.) 14:00-15:40

[P2-59]

Physics-Informed Optimisation of Conveyor Mode Spin Qubit Transport

Andrii Sokolov[1], Conor Power[1], Mathieu Moras[2], Claude Rohrbacher[2], Sergey Amitonov[3], Agostino Aprà[3], Amir Sammak[3], Nodar Samkharadze[3], and Elena Blokhina[1]
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[2]*Equal1 Laboratories, Sherbrooke, J1K 1B7, Canada*
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Scalable quantum information processing in spin-based architectures necessitates the ability to reliably shuttle quantum states across extended device regions with minimal decoherence. This enables connectivity beyond static nearest neighbours. Our approach combines non-linear Poisson and Schrodinger solvers to maintain a constant ground-state energy and enable near-constant-velocity shuttling, with potential applicability to both single-electron and hole transport [1].

Building on our previous simulation work, we present results of our multi-physics framework using a Silicon-Germanium Heterostracture (Si/SiGe), highlighting key limitations and material-specific effects [2] that influence transport fidelity. The main goal of this work is to calculate the limiting speed and acceleration of conveyor-mode shuttling in the presence of a number of non-idealities, including a physically derived valley splitting landscape and dephasing due to stray micromagnet fields over the silicon channel. We compute the Landau-Zener criteria under an adiabatic assumption from time-independent wavefunctions and include results from our time-dependent solver for estimation of non-adiabatic effects. Our core motivation is to understand the impact of valleys and magnetic field dephasing on shuttling fidelity, where our previous work demonstrated the generation of waveforms for constant velocity shuttling.

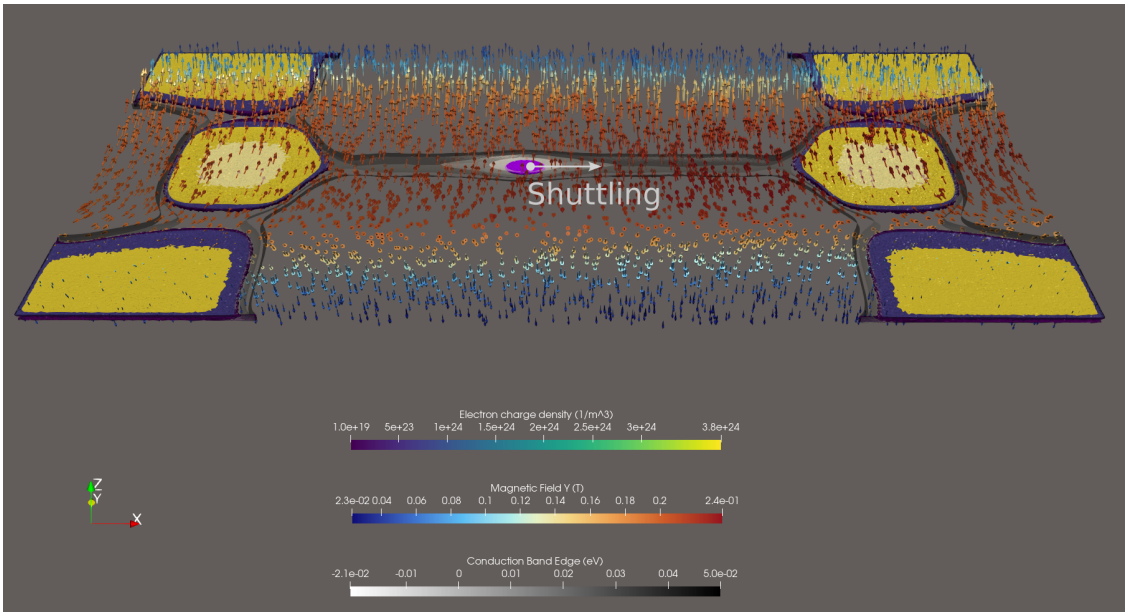

Figure 1. An example of conveyor mode shuttling in Si/SiGe device in the presence of a realistic external magnetic field.

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Poster | September 1 (Tue.) 14:00-15:40

[P2-60]

Lifted Product Quantum LDPC Codes with Reduced Connectivity for Silicon Quantum Dots

Gözde Üstün[1], Anantha Rao [1] and Michael J Gullans [1]

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Low-density parity-check (LDPC) codes are classical binary error-correcting codes[1] that underpin modern silicon-based solid-state devices and storage technologies as well as networking systems[2].
In recent years, a fundamental question has emerged: can quantum LDPC (QLDPC) codes be constructed directly from classical binary codes? Although the answer is not straightforward, it is indeed possible to build QLDPC codes from classical codes. A well-known approach is the hypergraph product construction[3], which typically yields codes with low code rates—defined as the ratio of logical to physical qubits—as well as long-range connectivity that is often considered impractical for realistic hardware implementations (yet it is more resource efficient compared to the surface code). More recently, an alternative construction known as "lifted product codes" has been introduced[4]. This approach is based on engineering a protograph, namely a structured matrix whose elements are shifted identity matrices. Lifted product codes can achieve significantly higher code rates while substantially reducing long-range connectivity. In this work, we focus on designing protographs that minimize long-range interactions and tailoring them for silicon quantum dot hardware. To efficiently implement these optimized codes on silicon quantum dots equipped with qubit shuttling, we further optimize the chip layout by identifying geometries that minimize shuttling-induced noise for a given set of parity checks. Our preliminary results show that lifted product codes can be efficiently implemented on silicon quantum dots without the need for long-distance qubit shuttling, enabled by both careful silicon chip architecture design and judicious choices of protographs.

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Poster | September 1 (Tue.) 14:00-15:40

[P2-61]

Design and fabrication of Si/SiGe-based qubit devices for developing middle-range shuttling

Gen Nakagawa, Shogo Fujita, Kenichiro Senda, Tatsuo Tsuzuki, Hideaki Yuta, Chinnasamy Rajkumar, Kotaro Taga, Rio Fukai, Akira Oiwa, and Takafumi Fujita

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Middle-range shuttling technologies have been reported that they can transport electrons over distances as long as 10 μm [1]. In addition, concepts for scaling up these systems using conveyors with non-linear geometries, such as T-junction structures [2], have also been proposed, and their practical implementation is highly desired.

In this work, we present the current status and measurement results of device development using Si/SiGe substrates in our laboratory, as well as simulations of T-junction shuttling. Toward systematically identifying the causes of decoherence during shuttling, we plan to fabricate multiple devices with different structural parameters and investigate the dependence on device structure. As a first step, we will analyze the effects of surface treatment on the surface of Hall bar devices fabricated on Si/SiGe substrates using C–V measurements. In addition, we will fabricate dot devices on Si/SiGe substrates and perform small-scale shuttling experiments. By comparing the electrode widths, gate pitches, gate voltages, and shuttling conditions determined based on simulations with the results obtained from actual devices, we aim to establish design criteria and control parameters for fabricating shuttling devices.

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Poster | September 1 (Tue.) 14:00-15:40

[P2-62]

Bayesian Optimization of High-Fidelity Spin Shuttling in Straight Channels and T-Junctions

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We develop a theoretical and numerical framework for designing high-fidelity, high-speed electron-shuttling protocols applicable to both straight channels and T-junctions [1], while explicitly accounting for the time-dependent in-plane confinement strength. In this work, we focus on the ideal noise-free limit to clarify the intrinsic speed-fidelity trade-off, with particular emphasis on accelerating shuttling through T-junctions.

The T-junction geometry modifies the confinement potential and the corresponding orbital wave functions, making high-fidelity transport at high speed more challenging than in straight channels. These geometric changes alter the effective matrix elements of the spin-orbit coupling Hamiltonian and the valley-orbit coupling matrix element, thereby modifying the valley splitting [2]. This effect does not originate from a change in the intrinsic spin-orbit coupling coefficient itself, but rather from changes in the effective coupling mediated by the modified confinement.

We construct the full Hamiltonian including excited orbital states along the x, y, and z directions [3], and numerically evaluate the shuttling fidelity using a time-dependent Schrieffer-Wolff transformation. To efficiently identify optimal control protocols, we employ Bayesian optimization to jointly optimize the electron velocity and the time-dependent in-plane confinement-strength profile. Our results provide a route toward fast T-junction shuttling protocols that maintain high fidelity under ideal noise-free conditions.

References

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International Conference on Spin Shuttling 2026

ICOSS 2026

September 3 (Thu.)

Songdo ConvensiA, Incheon, Korea